REMARKS

Claims 1-14 are currently pending in the above-identified application. Claims 1, 3, 5, 6, 7, 8, 10, 12, 13, and 14 are independent. Claims 8-14 have been added.

Information Disclosure Statement

Applicants have found a typographical error in the citation of a reference listed on the Form 1449 filed May 24, 2001. In particular, in the reference "KARRAFALT J. et al.," the name of the conference proceeding should be corrected to . "2ND IEEE INTERNATIONAL WORKSHOP OF TESTING EMBEDDED CORE-BASED SYSTEM CHIPS." Please make the appropriate correction for this citation.

Drawings

The drawings have been objected to. Accordingly, corrected formal drawings for Figures 1, 3, 5 and 7 are provided herewith.

Title

The title has been objected to as not being descriptive. Accordingly, the title has been replaced.

Claim Rejection – 35 U.S.C. 102

Claims 1 and 2 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by Brown et al. (U.S. Patent 5,627,842). Applicants respectfully traverse this rejection.

Summary of the Present Invention

The present invention, in a preferred embodiment, is directed to a semiconductor device having a plurality of semiconductor integrated circuit chips which are integrally sealed. In order to accommodate boundary scan testing, a set of pins are provided for external connection of the semiconductor device and each chip is subsequently internally connected by wires. Thus, since each integrated circuit chip does not have its own set of pins, the overall number of pins is reduced. Thus, testing can be carried out for the integrally sealed integrated circuit chips, but in a smaller package.

The present invention improves over previous designs to accommodate boundary scan testing of a multiplicity of integrated circuit chips that, for example, arranged the chips on a substrate and connected test pins of each chip to a common connector (see for example Figure 7, showing a connector 12 connected to associated pins of each chip, arranged on substrate 11). In the present invention, in a preferred embodiment, integrated circuits having pad interfaces are stacked on a pad substrate (e.g., see arrangement in Figure 2). External connections

for the set of integrated circuits is provided by a plurality of solder bumps formed on the pad substrate. Internal connections are provided by the printed substrate and wires connecting the integrated circuit chips. Thus, in the preferred embodiment, the total number of test pins for the set of integrated circuits is only five. Thus, the present invention uses fewer pins for testing a plurality of integrated circuit chips that in previous designs.

In an alternative embodiment, a pad for the signal line TDI of a subsequent integrated circuit is connected by a wire to pin BO. Pin BO corresponds to a signal line TDO of a preceding integrated circuit chip. Such a connection is provided in the case where integrated circuit chips cannot be connected to each other (e.g., Figure 4). Furthermore, given such an arrangement, it is possible to provide test commands using just the input pins, reducing the test pattern length (Specification, page 17, first full paragraph).

In a still further embodiment, TAPC 7, registers 3, 4, and 5 are not included in chips of second and subsequent stages. Instead the first chip is provided with relay lines TDIa and TDOa, and output signal lines TAP0 to TAP4. In such an arrangement, only the first chip is connected to the test signal input terminal, the test result output terminal, and to the control signal input terminals. Since the TAPC 7 and registers are shared among the chips, the number of gates on the chips is reduced, thereby further reducing total chip area (Specification, page 21, last paragraph).

Brown

Brown is directed to an apparatus and method for centralized boundary-scan fault-testing. Brown's invention is based on the IEEE Std 1149.1 standard. More specifically, Brown is directed to system-wide testing of a multiplicity of integrated circuit modules, e.g., as a plurality of printed circuit boards (column 1, lines 14-19). Brown discloses an example of a prior art test arrangement for a circuit module made up of a number of daisy-chained interconnected IC chips mounted on a circuit board (shown in Figure 2). In that arrangement, each chip contains a set of pins (Brown, column 3, lines 56-65).

Differences over Brown

The claimed invention, of claims 1 and 2, is directed to a semiconductor device comprising, among other things, a plurality of chips which are "integrally sealed." As mentioned above in the summary of the invention, an object of the present invention is to achieve a smaller semiconductor device of a plurality of integrated circuit chips, and to accommodate boundary-scan testing. The object is accomplished in the present invention by integrally sealing a plurality of integrated circuit chips and providing an external connection via a plurality of pins including the necessary test pins. The integrated circuit chips are connected to the test pins, such that they do not require there own test

pins, thus reducing the overall number of test pins and reducing the size of the package.

> Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. Dismissed, 468 U.S. 1228 (1984); W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. Denied, 469 U.S. 851 (1984).

Brown does not at least disclose a plurality of chips, "which are integrally sealed." Thus, at least for this reason, Brown does not anticipate the invention of claims 1 and 2. Accordingly, Applicants respectfully request that the rejection be withdrawn.

Claim Rejection – 35 U.S.C. 103

Claims 3-7 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. (U.S. Patent 5,627,842). Applicants respectfully traverse this rejection.

Claim 5 is directed to the same embodiment as in the above for claim 1. The Office Action admits that Brown does not explicitly teach only one of the chips connected to the test signal input terminal and test signal output terminal whereby the test signal is transferred to the other chips. However, as in the above for claim 1, Applicants submit, however,

that Brown does not disclose the claimed "semiconductor device in which a plurality of chips are integrally sealed." Based on the structure of the claimed invention, a semiconductor device of fewer pins and smaller size is provided. Brown is not concerned with providing a smaller semiconductor package. Thus, all elements of claim 5 are not taught or suggested by Brown.

Claims 3, 4, and 7 are directed to an embodiment (shown for example in Figure 5) wherein only one of the plurality of chips are connected to the test signal input terminal, the test result output terminal, and control signal input terminals, and a relay output terminal of the one chip of the first stage is connected to a terminal of a chip of a following stage.

The Office Action admits that Brown does not teach the limitation of a single chip connected to the test signal input terminal, test result output terminal and control signal input terminals, and the one chip successively transferring the test signal and test control signals through other chips. The Office Action instead alleges that Brown's techniques are similar to the applicants' method, such that it would have been obvious to one of ordinary skill in the art to modify Brown's invention to that of the present invention "in order to maximize the system's testing performance." Applicants disagree that techniques disclosed in Brown are similar to the claimed invention, such that the claimed invention would have been considered an obvious variation.

Brown, as addressed in the above for claim 1, does not teach or suggest a semiconductor device comprising a plurality of chips, which are integrally sealed. Furthermore, Brown does not disclose the claimed arrangement, and much less provide evidence that such an arrangement would maximize testing performance. In particular, Brown does not disclose "only one of said plurality of chips being connected to said test signal input terminal, to said test result output terminal, and to said control signal input terminals." Figure 2 of Brown, for example, shows control signal input terminals TCK and TMS connected to each of the integrated circuits. The arrangement of the present invention of claims 3, 4 and 7 was based on an object to reduce package size. As mentioned above, based on such an arrangement, the TAPC 7 and registers are shared among the chips, enabling chips with fewer numbers of gates, thereby further reducing total chip area as well as package size. Thus, Applicants submit that Brown does not teach or suggest all elements of the claimed invention of claims 3, 4 or 7.

Claim 6 is directed to an embodiment wherein integrally sealed chips are combined to front and rear surfaces of a substrate, such that there is no interconnection between chips (e.g., Figure 4). Rather, a test result output terminal of the semiconductor device is connected to a test input terminal of a chip of a flowing stage (e.g., WOI in Figure 3).

The Office Action again refers to the prior art device shown in Figure 2 of Brown. However, Applicants disagree that Brown teaches or

suggests the claimed invention of claim 6. As stated before, Brown does not disclose a semiconductor device in which a plurality of chips are integrally sealed. Furthermore, Applicants submit that Brown does not disclose "the test commands/data output terminal of each chip being connected to a corresponding output terminal of the device and serially to the test commands/data input terminal of a chip of a following stage via the output terminal of the device." The claimed arrangement enables a reduction in the test pattern length. Thus, Applicants submit that Brown fails to teach or suggest all claimed elements of claim 6.

Accordingly, Applicants submit that the rejection fails to establish *prima facie* obviousness for claims 3-7, and respectfully requests that the rejection be withdrawn.

New Claims

Claims 8-14 have been added to provide alternative ways of stating the claimed invention. For example, the new claims state that wires are sealed with the plurality of chips, and thereby serve as the connection medium between chips, and that terminals of the semiconductor device are "pins" while terminals of the chips are "pads." Such clarifications emphasize the distinction over the Brown reference which does not disclose integrally sealed chips and where each chip includes pins for all test signals.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 9-27, 32-37 and 40-43 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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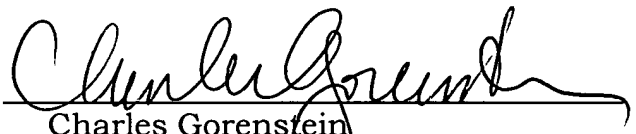
By: 

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